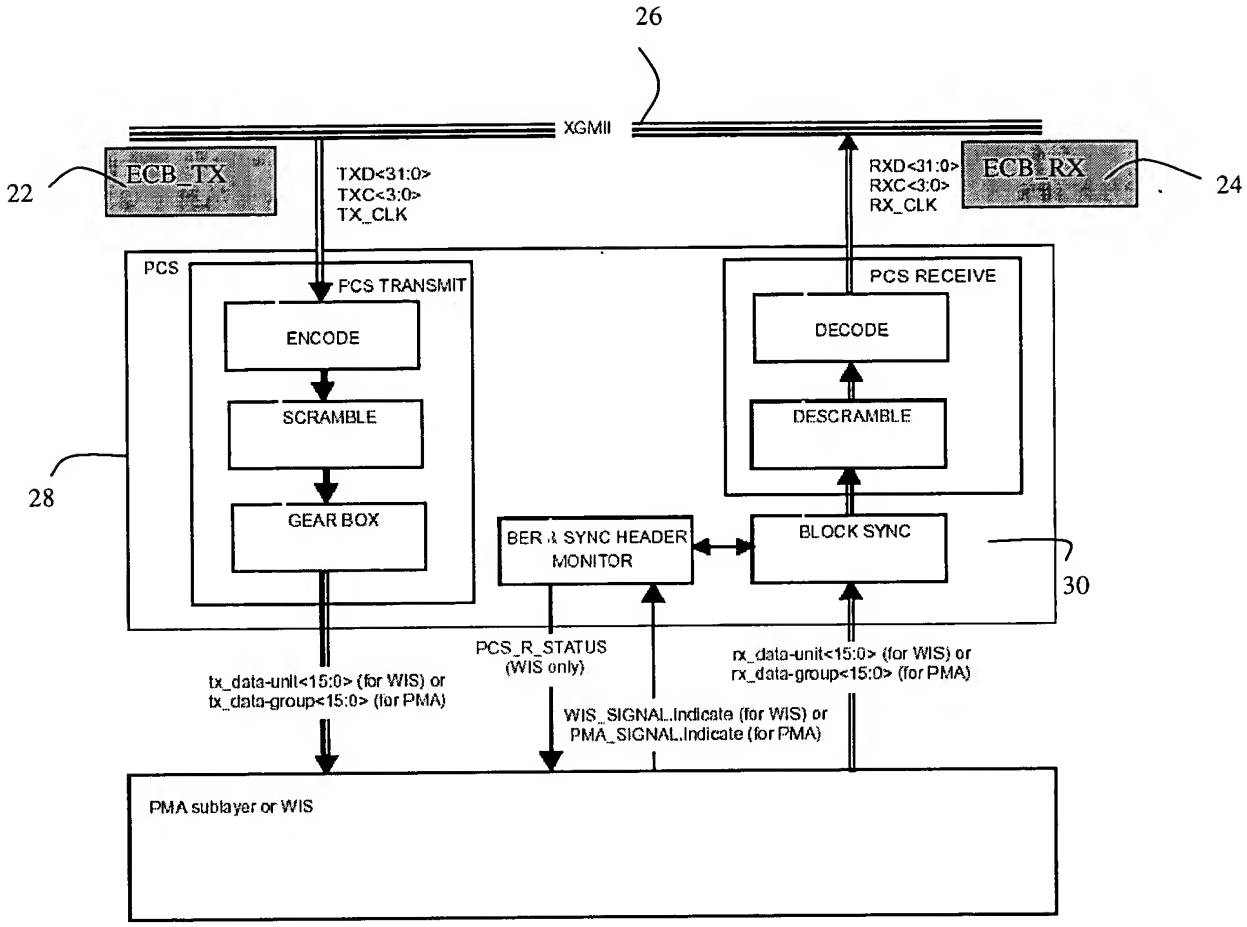

Figure 1: Functional Block Diagram of the PCS layer in 10GBASE-R Ethernet PHY.

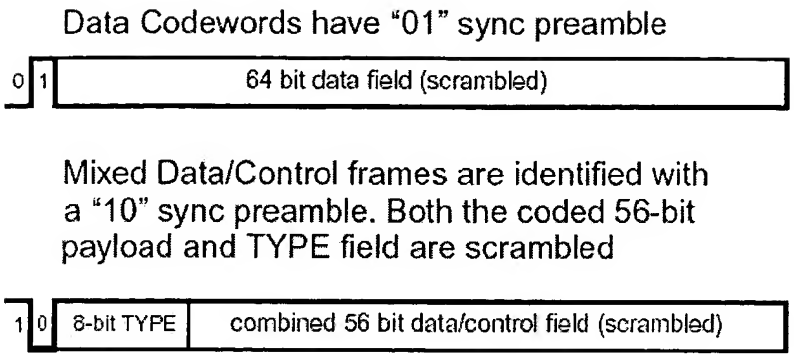

Figure 2: 64b/66b code words.

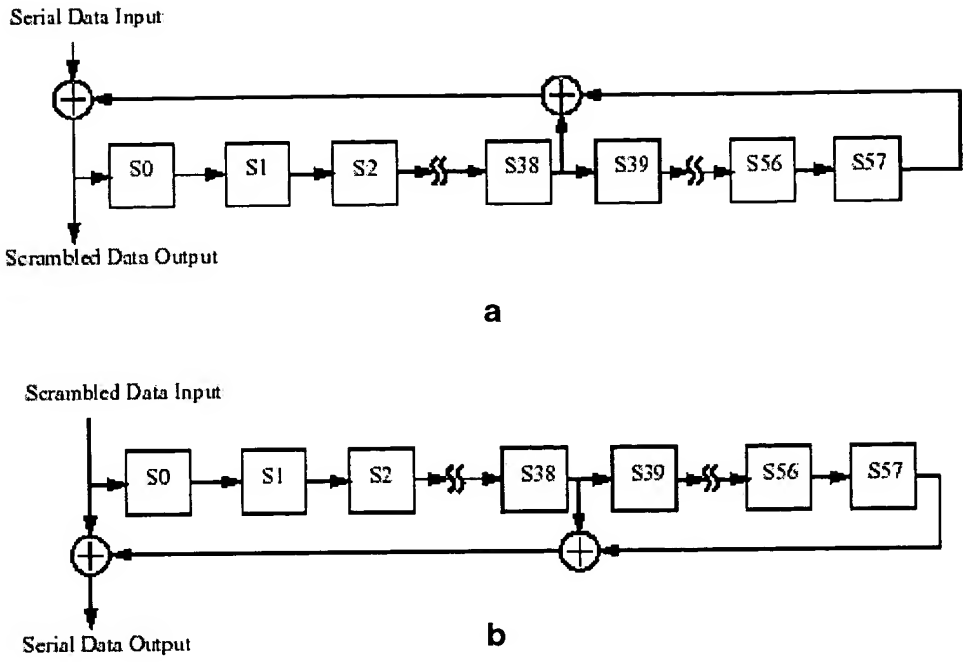

Figure 3: The self-synchronous scrambler and descrambler used in 64b/66b encoding.

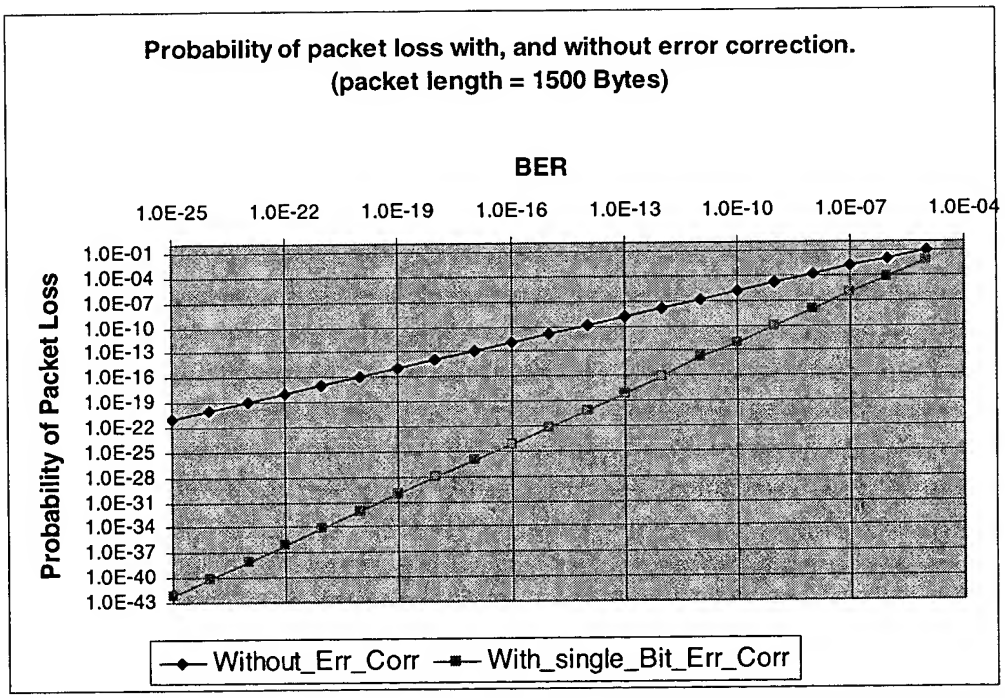

Figure 4: Probability of packet loss with, and without single-bit error correction.

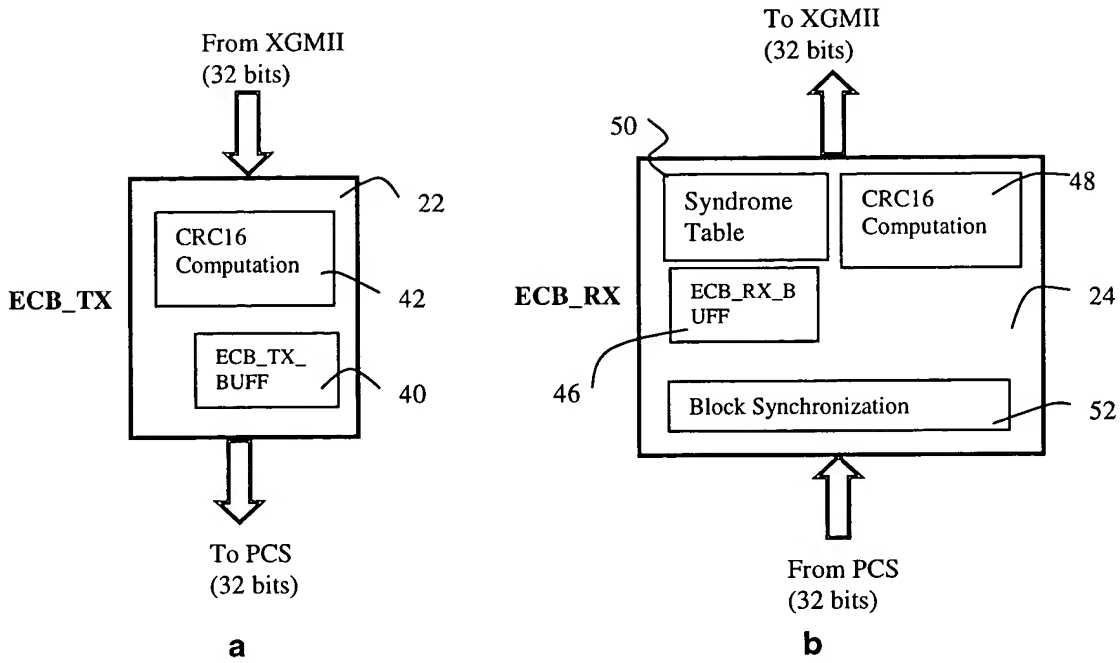

Figure 5: Functional block diagram of the Error Control Blocks (ECB).

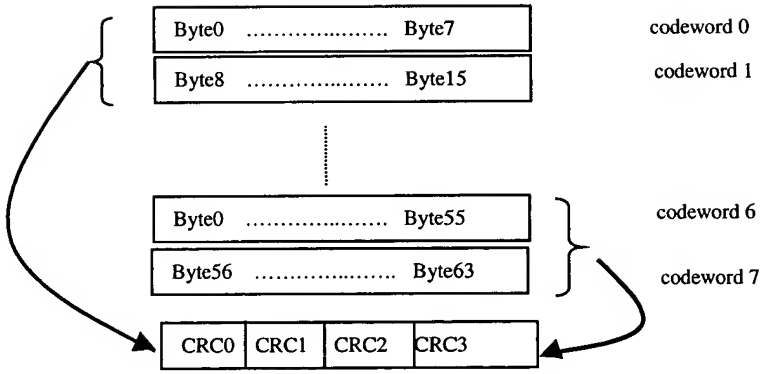

Figure 6: The buffer format in the ECB_RX and ECB_TX modules.

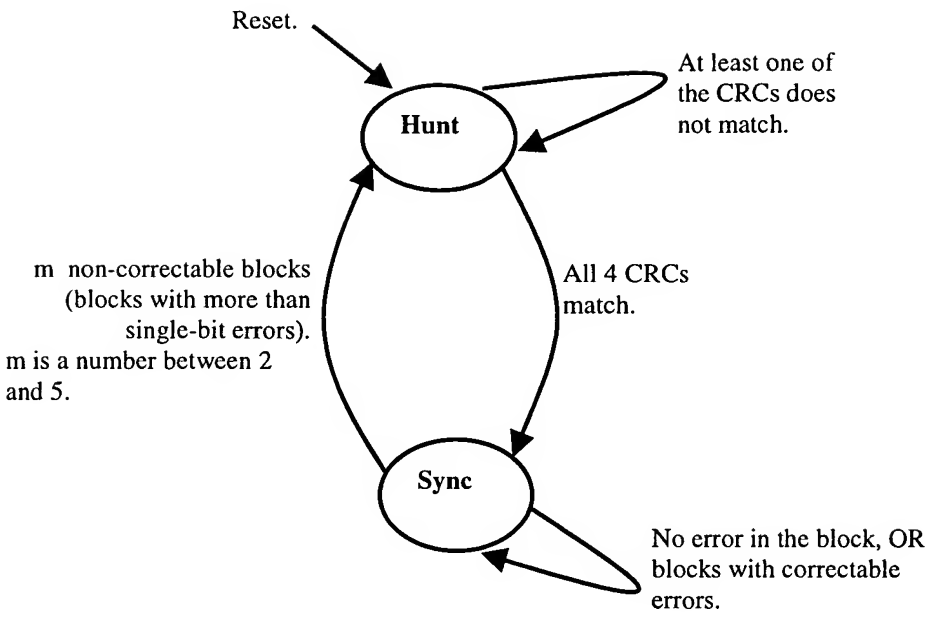

Figure 7: The state diagram of the block synchronization in the ECB_RX module.